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Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	Not assigned yet
				Filing Date	On even date herewith
				First Named Inventor	K. OSADA, et al.
				Art Unit	Not assigned yet
				Examiner Name	Not assigned yet
Sheet	1	of	1	Attorney Docket Number	500.35578CC5

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
H/H		5,253,207		10/93	Shikatani	
		5,675,529		10/97	Poolla	
		5,574,687		11/96	Nakase	
		5,517,462		05/96	Iwamoto et al	
		5,387,827		02/95	Yokoyama et al	
		5,535,172		07/96	Reddy et al	
		4,984,204		01/91	Sato et al	
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		5,657,286		08/97	Arimoto	
		5,570,319		10/96	Santori et al	
H/H		5,657,273		8/12/97	Ayukawa et al.	

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)					
H/H		4-65788		3/18/92			
		3-216892		8/24/91			
		3-3195		1/09/91			
		8-212776		8/96			
		2-50396		2/90			
H/H		7-201197		8/95			

OTHER PRIOR ART—NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published				T ²
H/H		Osada et al., "A 2ns Access, 285MHz, Two-Port Cache Macro Using Double Global Bit-Line Pairs" ISSCC Digest of Technical Papers, pp. 402-403				
H/H		Kushiyami et al., "A 295MHz CMOS 1M (x256) Embedded SRAM Using Bi-directional Read/Write Shared Sense Amps and Self-Timed Pulsed Word-Line Drivers" ISSCC Digest of Technical Papers, Feb. 1995, pp. 304-305				
H/H		IEEE Journal of Solid State Circuits, Vol. 23, No. 5, Oct. 1988, pp. 1048-1053				

Examiner Signature	17-HO	Date Considered	3/16/07
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